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Low Power and Low Dead Zone Phase Frequency Detector in PLL

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Abstract

This article presents Low power and Low Dead Zone Phase Frequency Detector for phase locked loop feedback system. It describes a design of a Phase Frequency Detector (PFD) using AND Gate and NOR Gate for 50 MHz and 500MHz frequency and also the comparative analysis of power dissipation and Dead Zone for 50MHz and 500MHz frequency. The Phase Frequency Detector is operated at 1.8V power supply. The proposed architecture of PFD has been implemented using 0.18µm CMOS Technology in ELDO- Mentor Graphics tool.

Keywords: Mentor Graphics; CMOS; DPLL; PFD

Introduction

Low jitter and Low power phase lock loop is becoming essential for portable and battery operated compact electronic devices, which decreases the risk of reliability problems. So power and jitter have been major concern in circuit designs from last decade. Now a day, the design of low power and low jitter PLL for the different application has become one of the greatest challenges task in high-performance very large scale integration (VLSI) design.

As a consequence, many techniques have been introduced to minimize the power and reduction in jitter of new VLSI circuits. A Phase Locked Loop also multiplies a low frequency reference clock signal, to produce a high frequency output clock signal. A PLL is a negative feedback control system. As the name implies, the main purpose of the PLL is to generate a signal in which the phase is the same as the phase of a reference clock signal. This is done after many iteration of comparing the reference and feedback signal. The overall goal of the PLL is to match the reference and feedback signal in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

A basic form of a PLL that consists of five main blocks:

1. Phase Frequency Detector (PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Network

The basic block diagram of the Phase Locked Loop feedback system is shown in figure 1.

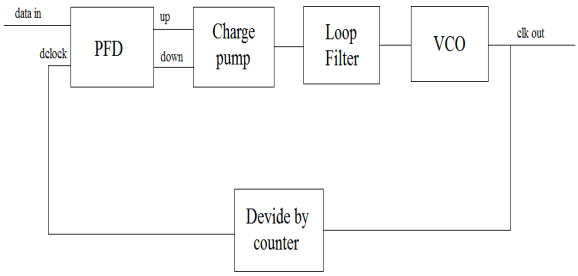

Figure 1: A Basic Block Diagram of Phase Locked Loop

As shown in figure 1, the phase frequency detector produce an error signal based on the phase differences between the phase of two input signal that is reference signal data in and the feedback clock signal dclock. If there is a phase difference between the two signals, it generates an error signal. This error signal drives the low pass filter, which increases or decreases the control voltage. This controlled voltage is the input of the Voltage Controlled Oscillator (VCO). Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge. The purpose of the VCO is to speed up or slow down the feedback signal according to the error generated by the PFD.

The average difference in time between the phases of the two Input reference and feedback

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signals when the PLL has achieved lock is called the static phase offset (steady-state phase error) and this variance is called jitter.

Power is a limiting factor in VLSI integration for portable applications. The resulting heat dissipation also limits the feasible packaging and performance of the VLSI chip [5]. Since the dynamic power dissipation in synchronous digital integrated circuit is determined by CV2f, reducing the supply voltage is an effective way to reduce power [4].

The paper is organized as follows. Section II contains design issues of phase frequency detector circuit and characterization. Section III contains of two phase frequency detector in two different technologies with detailed circuit diagram and simulated output. Section IV contains the table of specifications with results. Section V concludes the best PFD for low Dead Zone and low power PLL.

Design Issues

Dead zone is due to small phase error, when both the input signals of PFD are very close to each other but two output signals are not able to generate this error it will create the problem that is nothing but dead zone.

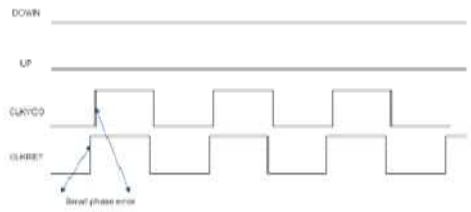

Fig.2 Dead Zone

Fig. 2 shows the lock condition of the PFD with dead zone. Dead zone is due to the delay time of the internal logic components of digital circuit and the reset time that requires by the reset path to reset the flip flop of the PFD. Due to this dead zone problem the output jitter will create and the sensitivity of the PFD is affected by this. In this case the sensitivity means the smallest phase difference the PFD can detect and produce at the output UP or DOWN signal. This lead to the conclusion that the higher the sensitivity the better the PFD.

Circuit Architecture of Phase Frequency Detector

A. PFD using AND Gate

A schematic diagram of the phase frequency detector using AND Gate is shown in the figure 3. The output of the PFD depends on both the phase and frequency of the inputs. This type of the phase frequency detector is also known as the sequential detector. Phase Frequency detector (PFD) is a digital circuit detecting phase or frequency difference between reference clock and output of voltage controlled oscillator (VCO) clock signal and generates output signal if frequency of VCO is to be increased or decreased. PFD drives the Charge Pump (CP) and adjust the amount of the current to be injected to or from the loop filter capacitor. If there is a phase difference between the two input signals, it generates up or down synchronized signals to the charge pump.

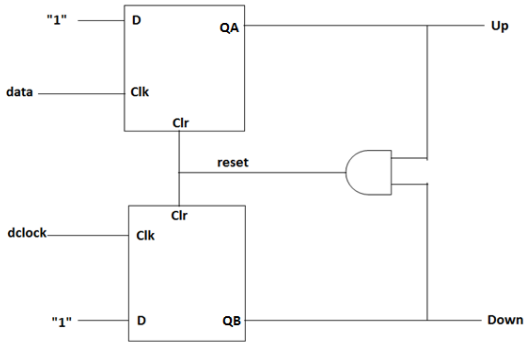

Figure 3: A Basic Block Diagram of Phase Frequency Detector

The operation of this circuit is based on two D-type flip- flop and simple AND gate in the reset path. Each flip-flop has the D-input wired logic high. Under this condition, the flip-flop with a low Q output will transition to high on the next rising edge of its clock input. Also if such a transition occurs when Q is high, then there will no change in the flip-flop state. A high signal on a reset input will force Q low as soon as the reset signal is applied. Finally, logic high on both of the Q output causes the resetting of both the flip-flops. The PFD generates two output signals that are not complementary to each other. The output signal depends not only on the phase error, but also on the frequency error. If the frequency, ω_A , of the input signal A is less than that of input signal B, ω_B, then the PFD produces positive pulses at Q_A, while Q_B remains zero. Same as, if $\omega_A > \omega_B$, then positive pulses appear at Q_B while Q_A remain zero. If $\omega_A = \omega_B$, then circuit generates pulses at either Q_A or Q_B with a width equal to the phase difference between the two inputs. so the average value of the Q_A - Q_B is proportional to the frequency or the phase difference between the inputs at data and dclock. The outputs Q_A and Q_B are called the up and down signals. The UP pulse is the difference between the phases of the two clock input signals. This UP pulse indicates that the feedback signal needs to speed up with the reference signal. In the second

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case, when the feedback signal is leading the reference clock signal, the DOWN pulse represents the difference between the phases of the two clock input signals.

The implementation of the PFD using AND Gate in the reset path with CMOS 0.18µm technology is as shown in the figure 4.The simulated output of this PFD is shown in figure 5. Simulation is done with the ELDO-MENTOR GRAPHICS TOOL

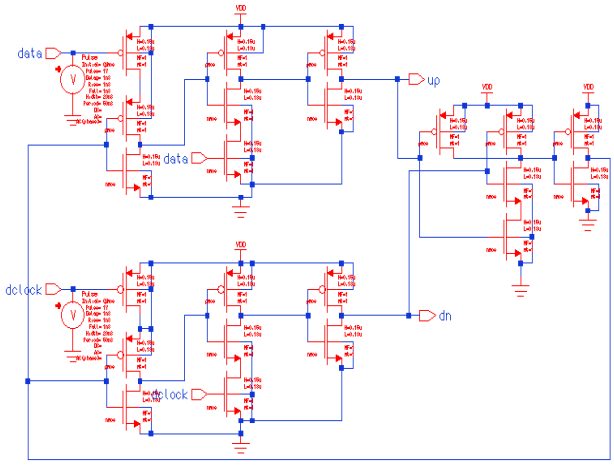

Figure 4: Implementation of Phase Frequency Detector

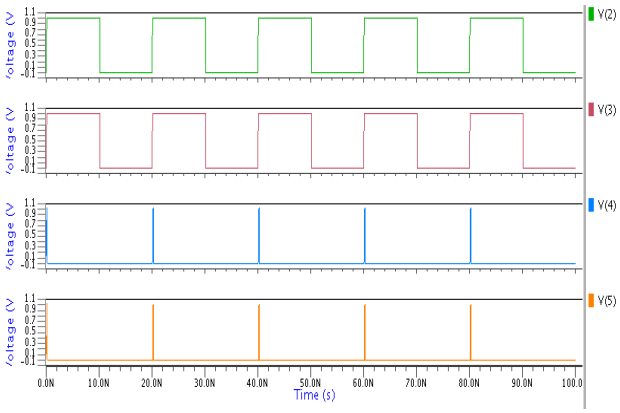

Figure 5: PFD at 50MHz (Lock Condition)

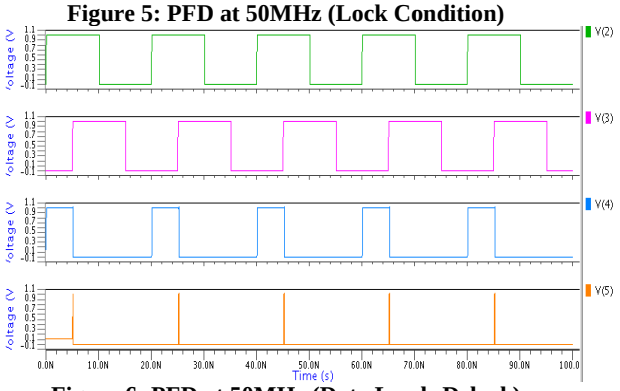

Figure 6: PFD at 50MHz (Data Leads Dclock)

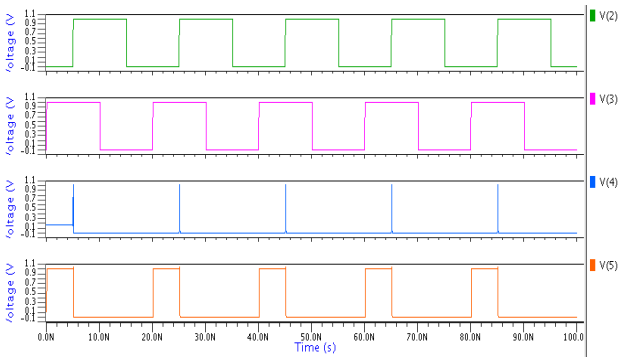

Figure 7: PFD at 50MHz (Dclock Leads Data)

Figure 5 shows, the lock condition of the PFD, both the output signals up and dn signals are low. Figure 6 and 7 the data leading condition and the dclock leading condition, the pulse width of the up signal or dn signal shows the relative value of the error generated between two inputs of the PFD. This error value is applied to the charge pump.

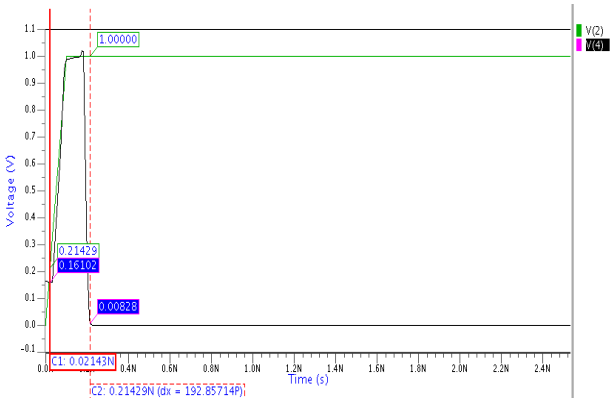

Figure 8: Dead Zone of the PFD (50MHz)

B. PFD using NOR Gate

In Fig.9 shows the PFD using NOR gate in reset path. The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NOR Gate in the reset path [3]. The data and dclock serve as clocks signal of the flip flops. The up and dn signals are given as input to the NOR gate in the reset path. When the rising edge of data leads that of dclock, then up goes to logic low i.e. UP keeps high until the rising edge of dclock makes dn on low level. Because up and dn are NORed, so RESET goes to logic high and resets the PFD into the initial state

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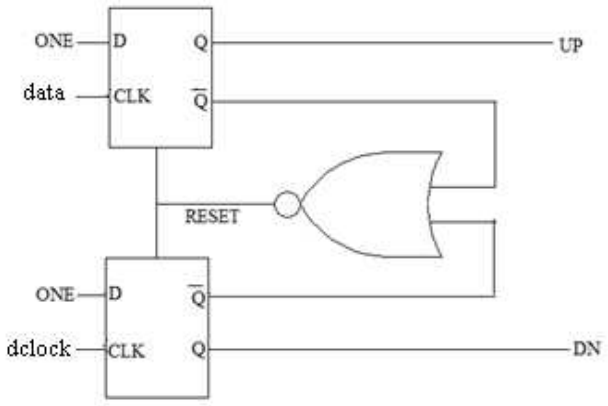

Fig.9 NOR Gate based PFD

The implementation of the PFD using NOR Gate in the reset path with CMOS 0.18µm technology is as shown in the figure 10.The simulated output of this PFD is shown in figure 11. Simulation is done with the ELDO-MENTOR GRAPHICS TOOL

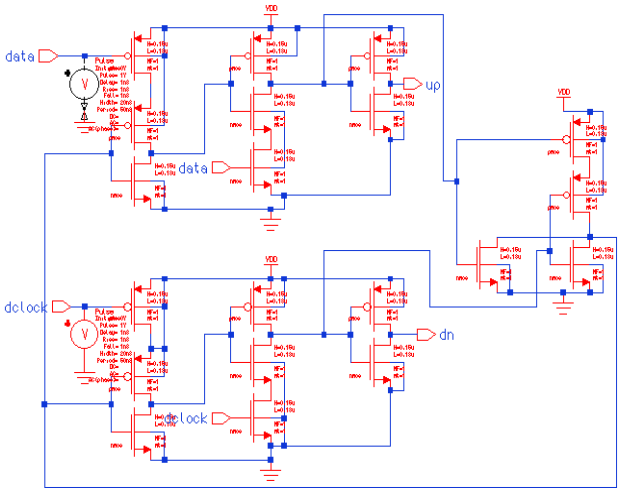

Figure:10 implementation of NOR Gate PFD

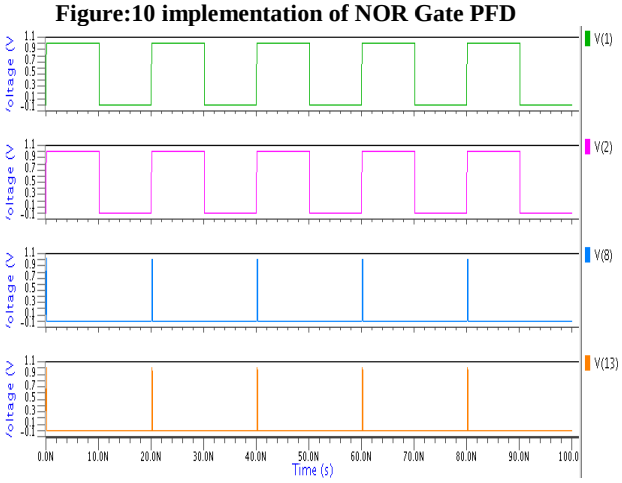

Figure 11: PFD at 50MHz (Lock Condition)

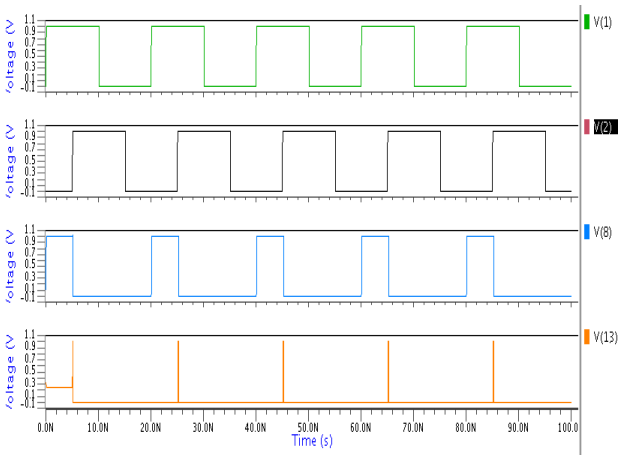

Figure 12: PFD at 50MHz (Data Leads Dclock)

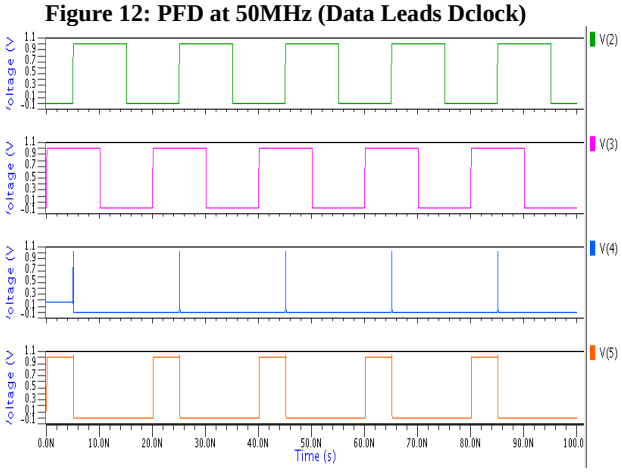

Figure 13: PFD at 50MHz (Data Leads Dclock)

Figure 10 shows, the lock condition of the NOR Gate PFD, both the output signals UP and DWN signals are low. Figure 11 and 12 the data leading condition and the dclock leading condition, the pulse width of the UP signal or DN signal shows the relative value of the error generated between two inputs of the PFD. This error value is applied to the charge pump.

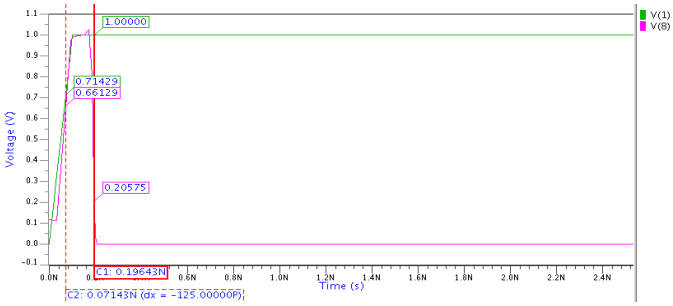

Figure 14: Dead Zone of the NOR Gate PFD (50MHz)

As shown in figure 13, the Dead Zone of NOR Gate PFD is 125ps At 50 MHz Frequency

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Simulation Result

Parameter	NOR Based PFD	AND Based PFD	NOR Based PFD	AND Based PFD
Technology	0.18µm	0.18µm	0.9µm	0.9µm
Input Frequency	50MHz	50MHz	50MHz	50MHz
Transistor count	20	22	20	22
Power Consumption	3.0715 E-04 WATTS	3.7672 E-04 WATTS	3.0588 E-04 WATTS	3.4746 E-04 WATTS
Dead zone	300ps	321ps	125ps	192ps
Glitch Period	375ps	468.75 ps	182.22 ps	200ps

Table 1: Comparison of Jitter and Power Dissipation of PFD at 50MHz frequency

Parameter	NOR Based PFD	AND Based PFD	NOR Based PFD	AND Based PFD
Technology	0.18µm	0.18µm	0.9µm	0.9µm
Input Frequency	500MHz	500MHz	500MHz	500MHz
Transistor count	20	22	20	22
Power Consumption	4.8162 E-04 WATTS	5.2995 E-04 WATTS	4.2117 E-04 WATTS	4.5209 E-04 WATTS
Dead zone	273.23 ps	292.95 ps	78ps	87ps
Glitch Period	281ps	359.15 ps	85.71ps	94.42ps

Table 2: Comparison of Jitter and Power Dissipation of PFD at 500MHz frequency

Conclusion

A Phase Frequency Detector with NOR Gate and AND Gate in the reset path is designed with 0.18µm CMOS technology, 1.8v power supply, 50 MHz and 500MHz input frequency. The Dead Zone of the AND Gate and NOR Gate design is 87ps and 78ps at 500MHz frequency. The total power dissipation of the AND Gate and NOR Gate circuit is 0.42mwatt and 0.45mwatt.so NOR Gate PFD Is best for PLL because it has low Dead Zone and low power consumption. This paper has represented comparative analysis of different frequencies for jitter and power dissipation.

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